REMARKS

These remarks are in response to the Final Office Action mailed January 12, 2007 (Office Action). As this reply is timely filed, no fee is believed due. Independent claims 1, 11, 16, and 18 have been amended to clarify various aspects of the present invention. Dependent claims 2-5, 7, 9, 14, 17, and 19 have been amended to better conform to the amendments made to the underlying independent claims. No new matter has been introduced.

Claims 1-13 and 16-20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,345,378 to Joly et al. (Joly) in view of U.S. Patent No. 6,374,205 to Kuribayashi et al. (Kuribayashi). The Applicants respectfully disagree for the reasons set forth below.

Claims 1, 16, and 18 recite a limitation that "identify[ies] objects specific to the target architecture that are repeated to identify potential dummy objects". Joly fails to teach or suggest this feature. The cited portions of Joly relate to processing a circuit design, e.g., creating synthesis shells for a circuit design that can be synthesized to implement the circuit design. Joly does not teach or suggest that repeated objects specific to the target hardware architecture can be identified to identify potential dummy objects.

The Office Action appears to draw a comparison between the dummy objects recited in claims 1, 11, 16, and 18 of the present invention and the dummy cells taught be Joly. The dummy cells discussed by Joly specify an area attribute intended to compensate for the area previously occupied by gates removed during creation of synthesis shells. The dummy cells of Joly are instantiated as part of the synthesis shells during synthesis. By comparison, the dummy objects recited in the claims of the present invention are simulated and not synthesized. As such, the dummy cells of Joly and the dummy objects recited in claims 1, 11, 16, and 18 are unrelated.

Claims 1, 16, and 18 also recite a limitation that "create[s] a list of objects, from the netlist of objects, that are used by a circuit design to be implemented in the target hardware architecture". Claim 11 includes a similar feature in which a file is parsed "to extract a list containing object names for all used objects for the target architecture". Again, Joly teaches a technique for processing a circuit design for synthesis, but does

not disclose the creation of a list of objects from the netlist of the target hardware architecture used by a circuit design that is to be implemented in the target hardware architecture.

Claims 1, 16, and 18, recite a further limitation that "form[s] a list of unused objects in the target hardware architecture from the netlist of objects and the list of objects used by the circuit design". The Office Action asserts that Joly teaches this feature of the independent claims as well. Joly, however, is silent in this regard. Nowhere does Joly teach or suggest that a list of unused objects of the target hardware architecture can be formed from the netlist of objects of the target hardware architecture and the list of objects used by the circuit design.

Each of the limitations discussed above with respect to the independent claims of the present invention is distinct. The limitations recite three distinct types of "lists", e.g, a netlist of objects of the target hardware architecture, a list of objects used by the circuit design to be implemented on the target hardware architecture, and a list of unused objects of the target hardware architecture. Many of the passages of Joly that have been cited in the Office Action have been asserted against more than one of these limitations.

For example, FIGs. 3-7 and column 4, lines 46-67 have been cited for teaching objects of the target hardware architecture that are repeated, objects of the circuit design, and objects of the target hardware architecture that are unused. Similarly, column 6, lines 33-50 have been cited as teaching objects of the target hardware architecture that are repeated, objects of the circuit design to be implemented on the target hardware architecture, and unused objects of the target hardware architecture. Colum 10, lines 1-33 have been cited as teaching both objects of the target hardware architecture that are repeated and objects of the target hardware architecture that are not used by the circuit design.

By asserting that a given passage of Joly teaches multiple, distinct features recited by the Applicants' claims, the Office Action is ascribing a plurality of different meanings to a single passage. The Office Action is contending that a single passage of Joly teaches a netlist of objects for the target hardware architecture, a list of objects from the netlist that are used by the circuit design, as well as a list of objects of the

target hardware architecture not used by the circuit design. This is simply not the case and misconstrues the teachings of Joly. Moreover, it does not address the details recited in the independent claims. As noted, Joly lacks any teaching or suggestion regarding the creation of a list of objects from the netlist that are used by the circuit design or the creation of a list of objects of the target hardware architecture that are not used by the circuit design.

Claims 1, 11, 16, and 18 also recite a limitation that "replace[s] at least one object in the netlist of objects for the target architecture that is also specified in the list of unused objects with an appropriate dummy object to form a modified netlist". As noted, Joly teaches a method of processing a circuit design for synthesis. The methodology selectively removes internal gates from a gate level circuit description. The gates that are removed from the circuit description are "used" as indicated by the fact that the gates initially are part of the circuit design (gate level netlist) that is being synthesized. By comparison, the present invention replaces at least one object in the netlist of objects for the target architecture that is unused by the circuit design with a dummy object. The object of the target hardware architecture that is replaced by the dummy object is not part of the circuit design, but rather a part of the target hardware architecture that still is simulated despite not being part of the circuit design.

Claims 1, 11, 16, and 18 further recite a limitation that "simulate[s] the modified netlist". That is, the modified netlist of the target hardware architecture, including at least one dummy object, is simulated. As noted, the dummy objects of the present invention are simulated. The dummy cells of Joly are synthesized, not simulated. In fact, Joly is silent regarding simulation or processing a netlist for purposes of simulation. Simulating the modified netlist, in the case of an FPGA, for example, entails simulating all objects of the target hardware architecture. Replacing objects of the target hardware architecture not used by the circuit design with dummy objects effectively removes the unused blocks from simulation thereby condensing the netlist to be simulated. (*See* paragraph 18).

The Office Action concedes that Joly fails to teach or suggest the step of simulating the modified netlist. It is asserted that Kuribayashi teaches this step. Kuribayashi, however, fails to cure the deficiencies of Joly. The entirety of the Joly

specification is directed to synthesizing a netlist. Kuribayashi, unlike Joly, is directed to simulation. Joly does not mention simulation as a goal, a concern, or at all. Indeed, there is no teaching or suggestion from Joly that the use of synthesis shells and dummy cells would be workable, or even functional, in the context of simulation. With this in mind, one attempting to solve the issues addressed by the Applicants' invention, e.g., simulation, would not turn to Joly, a reference dealing with synthesis, for a solution. Moreover, this demonstrates a lack of motivation to combine the teachings of Joly with those of Kuribayashi.

Claims 8 and 12 teach the step of "feeding through a signal unchanged when simulating the appropriate dummy object during a simulation process using the modified netlist". Since the Office Action concedes that Joly does not teach simulating a modified netlist (which specifies at least one dummy object), Joly cannot teach or suggest either of these claims.

Relying in part upon Joly and Kuribayashi, claims 14 and 15 also have been rejected under 35 U.S.C. § 103(a). Accordingly, the remarks made in support of claims 1, 11, 16, and 18 are applicable here. While claims 14 and 15 are believed to be allowable on their own merits, both claims are allowable by virtue of their dependency upon independent claim 11. In addition, with respect to claim 14, U.S. Patent No. 6,173,343 to Wirthlin, et al. (Wirthlin), like Joly, relates to implementation of a circuit design and, more particularly, to a reconfigurable processor. Wirthlin is unrelated to simulation. As such, there is no motivation to combine the teachings of Joly, Kuribayashi, and Wirthlin.

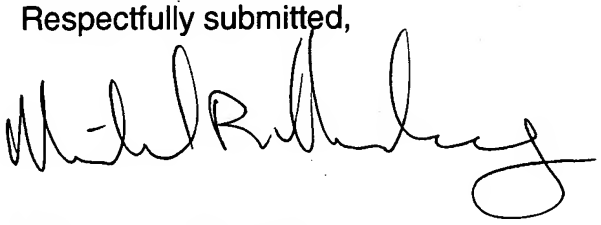
As neither Joly, Kuribayashi, nor any combination thereof teaches or suggests the Applicants' invention as claimed, withdrawal of the 35 U.S.C. § 103(a) rejection with respect to claims 1-20 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-7710.

Respectfully submitted,



Michael R. Hardaway
Attorney for Applicants
Reg. No. 52,992

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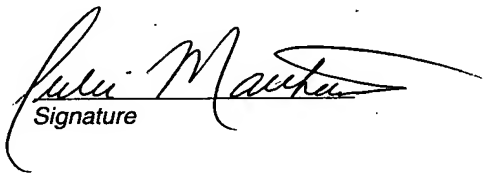
Name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